REMARKS

Applicants thank the Examiner for acknowledging receipt of Applicants' foreign priority document, Japanese Application No. 2000-290259, that has been submitted pursuant to 35 U.S.C. section 119. Applicants also thank the Examiner for accepting the proposed drawing changes as well as the arguments for patentability over the Jang Patent Nos. 6,165,915 and 6,180,540 set forth in the previous amendment, Amendment A.

Applicants have amended the abstract as requested by the Examiner. Applicants also submit that the previously amended claims 1-3 comport with all the requirements of Section 112 because "at least 10%" is implicitly disclosed in the specification. The Specification discloses that the FSG layer 13 is formed at a temperature 380°C and the NSG layer is formed at a temperate of 430°C. See specification, pages 7-8. Therefore, the NSG layer is formed at a temperature that is 50°C higher, at least 10% higher, than the FSG layer formation temperature. Accordingly, Applicants request that the Examiner withdraw these objections and rejections.

Applicants respectfully request reconsideration of the prior art rejection set forth by the Examiner under 35 U.S.C. § 102. Applicants respectfully submit that the prior art references of record whether considered alone, or in combination, fail to either teach or suggest Applicants' presently claimed invention.

Applicants' claimed invention is directed to improved methods for manufacturing semiconductor devices. More specifically, Applicants' claimed invention is directed to a method for producing a semiconductor device having a fluorine-doped silicon oxide layer as well as a silicon oxide layer formed over the fluorine-doped silicon oxide layer. Advantageously, Applicants have discovered that significant improvements over prior art techniques can be achieved by additionally and selectively removing a surface layer of the fluorine-doped silicon oxide layer by sputtering. For example, the Specification discloses

that about 100 nm of the surface layer of the FSG layer 13 is removed after the formation of the FSG layer 13 and prior to formation of the insulating layer. See page 11, lines 29-32. Subsequently, the silicon oxide layer is formed after the formation of the FSG layer. See generally page 12, lines 8-13.

Applicants note that the prior art cited by the Examiner, the Abdelgadir et al U.S. Patent No. 6,274,933, is directed to an integrated circuit device having the FSG layer. Abdelgadir et al merely discloses that during the SiO_2 formation step, argon simultaneously sputters away deposited materials. See Column 4, lines 34-42. This sputtering is merely incidental to the formation of the SiO_2. However, the present significantly improves and is patentably distinct from this prior art technique by requiring an additional step of removing a surface layer of the FSG layer after the formation of the FSG layer and prior to formation of the insulating layer. Thereafter, the silicon oxide layer and the P-TEOS layers are formed. See generally page 12, lines 8-13. This additional step advantageously eliminates or significantly reduces the fluorine impurities that result from prior art processes such as the process disclosed by Abdelgadir et al. Furthermore, this intentional selective removal is much better and more efficient than the prior art removal.

Abdelgadir et al does not achieve the advantageous benefits and characteristics of the semiconductor products that are manufactured in accordance with Applicants' claimed manufacturing techniques. Consequently, there is simply no teaching or suggestion whatsoever regarding Applicants' claimed manufacturing techniques which rely upon additionally sputtering away a surface layer of the FSG layer.

Accordingly, Applicants' invention is patentability distinct over the art of record. In light of the foregoing, Applicants respectfully submit that all claims now stand in condition for allowance.

Respectfully submitted,

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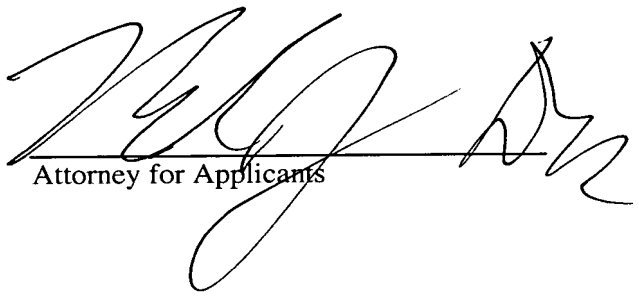

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